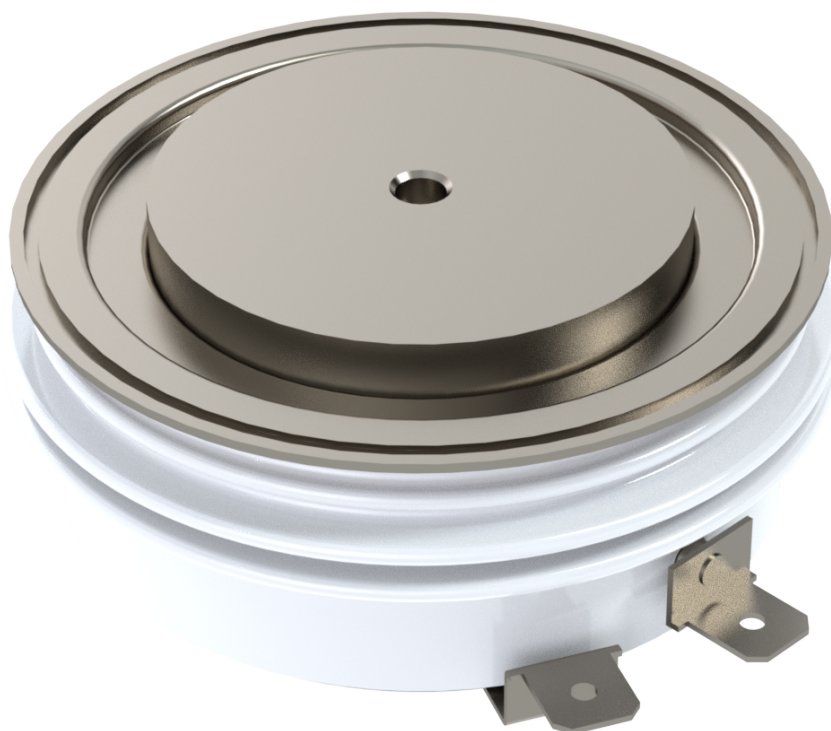


Anode Shorted Gate Turn-Off Thyristor Type SA25DP1000TB

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Date: July, 2020
Data Sheet Issue: 1



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SA	25	DP	1000	T	B	
-	Voltage Code	Outline Code	Current code	Type code	Special code	Optional code

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Absolute Maximum Ratings

VOLTAGE RATINGS		MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	4500	V
V_{RSM}	Non-repetitive peak off-state voltage, (note 1)	4500	V
V_{RRM}	Repetitive peak reverse voltage	18	V
V_{RSM}	Non-repetitive peak reverse voltage	18	V
$V_{DC-link}$	Maximum continuos DC-link voltage	2800	V
note 1)	$V_{GK} = -2V$		

OTHER RATINGS		MAXIMUM LIMITS	UNITS
I_{TGQ}	Peak turn-off current (note 1)	1000	A
L_S	Snubber loop impedance, $I_{TM} = I_{TGQ}$ (note 1)	300	nH
$I_{T(AV)M}$	Mean on-state current, $T_{sink} = 55^{\circ}C$, (note 2)	443	A
$I_{T(RMS)}$	Nominal RMS on-state current, $T_{sink} = 25^{\circ}C$ (note 2)	867	A
I_{TSM}	Peak non-repetitive surge current $t_p = 10ms$ (note 3)	6500	A
I_{TSM2}	Peak non-repetitive surge current $t_p = 2ms$ (note 3)	11450	A
I^2t	I^2t capacity for fusing $t_p = 10ms$	$211.25 \cdot 10^3$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current, (note 4)	300	$A/\mu s$
P_{FGM}	Peak forward gate power	185	W
P_{RGM}	Peark reverse gate power	7	kW
I_{FGM}	Peak forward gate current	100	A
V_{RGM}	Peak reverse gate voltage (note 5)	18	V
T_{jop}	Operating temperature range	-40 to +125	$^{\circ}C$
T_{stg}	Storage temperature range	-40 to +125	$^{\circ}C$
note 1)	$T_j = 125^{\circ}C$, $V_D = 2800V$, $V_{DM} \leq 4500V$, $di_{GQ}/dt = 25A/\mu s$, $I_{TGQ} = 1000A$ and $C_S = 1\mu F$		
note 2)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	$T_{j(initial)} = 125^{\circ}C$, single phase, 50Hz, 180° sinewave, re-applied voltage $V_D = V_R \leq 10V$		
note 4)	For $di/dt > 300A/\mu s$ please consult factory.		
note 5)	May exceed this value during turn-off avalanche period.		

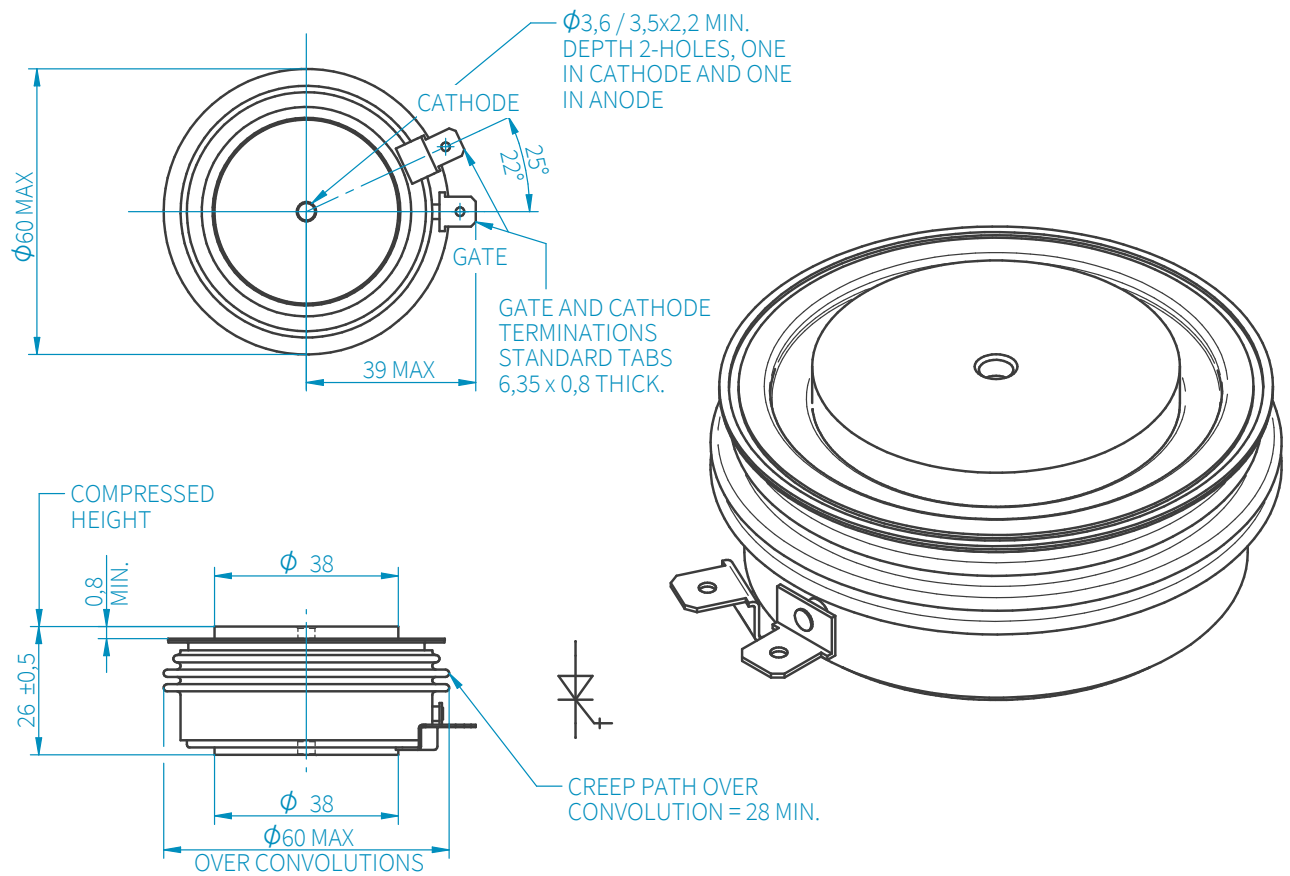
Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TM}	Maximum peak on-state voltage	$I_G = 2A, I_T = 1000A$	-	-	3.1	V
I_L	Latching current	$T_J = 25^\circ C$	-	40	-	A
I_H	Holding current	$T_J = 25^\circ C$	-	40	-	A
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	$V_D = 2800V, V_{GR} = -2V$	1000	-	-	V/ μs
I_{DRM}	Peak off-state current	Rated $V_{DRM}, V_{GR} = -2V$	-	-	60	mA
I_{RRM}	Peak reverse current	$V_{RR} = 16V$	-	-	20	mA
I_{GKM}	Peak negative gate leakage current	$V_{GR} = -16V$	-	-	20	mA
V_{GT}	Gate trigger voltage	$T_J = -40^\circ C, V_D = 25V, R_L = 25m\Omega$	-	1.0	-	V
		$T_J = 25^\circ C, V_D = 25V, R_L = 25m\Omega$	-	0.8	1.0	V
		$T_J = 125^\circ C, V_D = 25V, R_L = 25m\Omega$	-	0.6	-	V
I_{GT}	Gate trigger current	$T_J = -40^\circ C, V_D = 25V, R_L = 25m\Omega$	-	8	-	A
		$T_J = 25^\circ C, V_D = 25V, R_L = 25m\Omega$	-	-	5	A
		$T_J = 125^\circ C, V_D = 25V, R_L = 25m\Omega$	0.05	-	1	A
t_d	Delay time	$V_D = 1250V, I_{TGQ} = 2500A,$ $di_T/dt = 200A/\mu s, I_{GM} = 30A,$	-	0.7	2	μs
t_{gt}	Turn-on time	$di_G/dt = 20A/\mu s, C_S = 6\mu F, R_S = 5\Omega$	-	3	5	μs
t_f	Fall time		-	2	-	μs
t_{gq}	Turn-off time		-	-	30	μs
I_{GQ}	Peak turn-off gate current	$V_D = 1250V, V_{DM} = 2500V,$ $di_{GQ}/dt = 30A/\mu s, I_{TGQ} = 2500A,$	-	680	-	A
Q_{GQ}	Turn-off gate charge	$V_{GR} = -16V, C_S = 6\mu F$	-	9	-	mC
t_{tail}	Tail time		-	10	-	μs
t_{gw}	Gate off-time (note 2)		-	-	3.2	J
R_{thJK}	Thermal resistance, junction to sink	Double side cooled	-	20	-	K/kW
		Cathode side cooled	-	44	-	K/kW
		Anode side cooled	-	37	-	K/kW
F	Mounting force	(note 3)	21	-	26	kN
W_t	Weight		-	800	-	g
note 1)	Unless otherwise indicated $T_J = 125^\circ C$					
note 2)	t_{gw} is the period during which the gate circuit is required to remain at low impedance to allow for passage of tail current.					
note 3)	For other clamping forces, consult factory.					

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