Symmetrical Gate Turn-Off Thyristor Type SA25AP1200UL



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Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	2500	V
V_{RSM}	Non-repetitive peak off-state voltage, (note 1)	2600	V
V_{RRM}	Repetitive peak reverse voltage	1125	V
V_{RSM}	Non-repetitive peak reverse voltage	1125	V
note 1)	V _{GK} = -2V		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
I _{TGQ}	Peak turn-off current (note 1)	1200	А
L _S	Snubber loop impedance, $I_{TM} = I_{TGQ}$ (note 1)	0.3	μΗ
I _{T(AV)M}	Mean on-state current, T _{sink} = 55°C, (note 2)	670	А
I _{T(RMS)}	Nominal RMS on-state current, T _{sink} = 25°C (note 2)	1340	Α
I _{TSM}	Peak non-repetitive surge current t _p = 10ms	10.5	kA
I _{TSM2}	Peak non-repetitive surge current (note 3)	19	kA
l ² t	I^2 t capacity for fusing $t_p = 10$ ms	550 · 10 ³	A^2s
(di/dt) _{cr}	Critical rate of rise of on-state current, (note 4)	1000	A/µs
P _{FGM}	Peak forward gate power	210	W
P_{RGM}	Peark reverse gate power	8	kW
I _{FGM}	Peak forward gate current	140	А
V_{RGM}	Peak reverse gate voltage (note 5)	18	V
t _{off}	Minimum permissible off-time, $I_{TM} = I_{TGQ}$ (note 1)	80	μs
t _{on}	Minimum permissible off-time	20	μς
T _{jop}	Operating temperature range	-40 to +125	°C
T _{stg}	Storage temperature range	-40 to +150	°C
note 1)	$T_{j} = 125^{\circ}\text{C}, V_{D} = 80\%\text{V}_{DM}, V_{DM} \le \text{V}_{DRM}, \text{di}_{GQ}/\text{dt} = 20\text{A}/\mu\text{s}, C_{S} = 3\mu\text{F}$		
note 2)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Half-sinewave, t _p = 2ms		
note 4)	For di/dt > 1000A/μs please consult factory.		
note 5)	May exceed this value during turn-off avalanche period.		



Characteristics

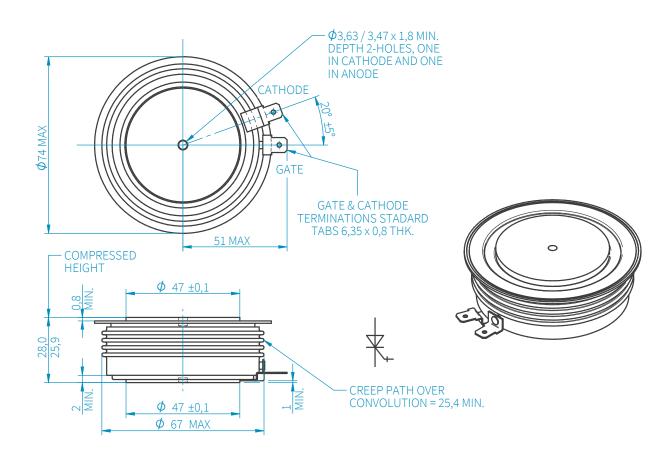
	PARAMETER	TEST CONDITIONS	MIN	TYP	мах	UNITS
V_{TM}	Maximum peak on-state voltage $I_G = 2A$, $I_T = 1200A$		-	3.0	3.3	V
IL	Latching current	T _i = 25°C	-	15	-	А
I _H	Holding current	1 _J = 25 C	-	15	-	Α
(dv/dt) _{cr}	Critical rate of rise of off-state voltage	$V_{D} = 80\%V_{DRM}, V_{GR} = -2V$	1000	-	-	V/µs
I _{DRM}	Peak off-state current	Rated V_{DRM} , $V_{GR} = -2V$	-	-	50	mA
I _{RRM}	Peak reverse current	Rated V _{RRM}	-	-	100	mA
I_{GKM}	Peak negative gate leakage current	$V_{GR} = -16V$	-	-	200	mA
		$T_j = -40^{\circ}C$, $V_D = 25V$, $R_L = 25m\Omega$	-	1.0	-	V
V_{GT}	Gate trigger voltage	$T_j = 25$ °C, $V_D = 25$ V, $R_L = 25$ m Ω	-	0.9	-	V
		$T_j = 125^{\circ}C, V_D = 25V, R_L = 25m\Omega$	-	0.8	-	V
		$T_j = -40^{\circ}C$, $V_D = 25V$, $R_L = 25m\Omega$	-	3.0	8.0	А
I_{GT}	Gate trigger current	$T_j = 25$ °C, $V_D = 25$ V, $R_L = 25$ m Ω	-	0.6	2.5	Α
		$T_j = 125$ °C, $V_D = 25V$, $R_L = 25m\Omega$	-	60	500	mA
t _d	Delay time	(note 2)	-	1.0	-	μs
t _{gt}	Turn-on time	Conditions as for $t_{\rm d}, (10\% l_{\rm GM}$ to $10\% V_{\rm D})$	-	3.0	7.0	μs
t _f	Fall time	(note 3)	-	0.8	-	μs
t _{gq}	Turn-off time	Conditions as for t_f , (10% I_{GQ} to 10% I_{TGQ})	-	12	13	μs
I_{GQ}	Turn-off gate current	Conditions as for t _f	-	250	-	А
Q_{GQ}	Turn-off gate charge	Conditions as for t	-	1600	2000	mC
t _{tail}	Tail time	Conditions as for t_f , (10% I_{TGQ} to I_{TGQ} < 1A)	-	40	60	μs
t _{gw}	Gate off-time (note 4)	Conditions as for t _f	150	-	-	μs
		Double side cooled	-	-	0.027	K/W
R_{thJK}	Thermal resistance, junction to sink	Cathode side cooled	-	-	0.070	K/W
		Anode side cooled	-	-	0.045	K/W
F	Mounting force	(note 5)	15	-	25	kN
W _t	Weight		-	480	-	g
note 1)	Unless otherwise indicated T _j = 125°C					
note 2)	$V_D = 50\% V_{DRM}$, $I_{TGQ} = 1200A$, $I_{GM} = 40A$, $di_G/dt = 20A/\mu s$, $T_j = 25^{\circ}C$, $di/dt = 300A/\mu s$, $(10\% I_{GM} to 90\% V_D)$					
note 3)	$V_D = 80\% V_{DRM}$, $I_{TGQ} = 1200A$, $C_S = 3\mu F$, $di_G/dt = 40A/\mu s$, $V_{GR} = -16V$, $(90\% I_{TGQ} \text{ to } 10\% V_D)$					
note 4)	The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the passage of tail current.					
note 5)	For other clamping forces, consult factory.					

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