Symmetrical Gate Turn-Off Thyristor Type SA20AP1200UD



Contact us!

Date: July, 2020 Data Sheet Issue: 1



ORDERING INFORMATION				(Please quote 12 to 15 digit code as below)			
SA	20	AP	1200	U	D		
-	Voltage Code	Outline Code	Current code	Type code	Special code	Optional code	



Explore the full range of our semiconductor portfolio online

SANCONA®

Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V _{DRM}	Repetitive peak off-state voltage, (note 1)	2000	V
V _{RSM}	Non-repetitive peak off-state voltage, (note 1)	2100	V
V _{RRM}	Repetitive peak reverse voltage	1600	V
V _{RSM}	Non-repetitive peak reverse voltage	1600	V
note 1)	$V_{GK} = -2V$		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
I _{TGQ}	Peak turn-off current (note 1)	1200	А
L _S	Snubber loop impedance, $I_{TM} = I_{TGQ}$ (note 1)	0.3	μΗ
I _{T(AV)M}	Mean on-state current, T _{sink} = 55°C, (note 2)	670	А
I _{T(RMS)}	Nominal RMS on-state current, T _{sink} = 25°C (note 2)	1340	А
I _{TSM}	Peak non-repetitive surge current t _p = 10ms	10.5	kA
I _{TSM2}	Peak non-repetitive surge current (note 3)	19	kA
l ² t	$I^{2}t$ capacity for fusing t_{p} = 10ms	$550 \cdot 10^{3}$	A ² s
(di/dt) _{cr}	Critical rate of rise of on-state current, (note 4)	1000	A/µs
P _{FGM}	Peak forward gate power	210	W
P _{RGM}	Peark reverse gate power	8	kW
I _{FGM}	Peak forward gate current	140	А
V _{RGM}	Peak reverse gate voltage (note 5)	18	V
t _{off}	Minimum permissible off-time, $I_{TM} = I_{TGQ}$ (note 1)	80	μs
t _{on}	Minimum permissible off-time	20	μs
T _{jop}	Operating temperature range	-40 to +125	°C
T _{stg}	Storage temperature range	-40 to +150	°C
note 1)	T_j = 125°C, V_D = 80% V_{DM} , V_{DM} ≤ V_{DRM} , di _{GQ} /dt = 20A/μs, C_S = 3μF		
note 2)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Half-sinewave, t _p = 2ms		
note 4)	For di/dt > 1000A/µs please consult factory.		
note 5)	May exceed this value during turn-off avalanche period.		

SANCONA®

Characteristics

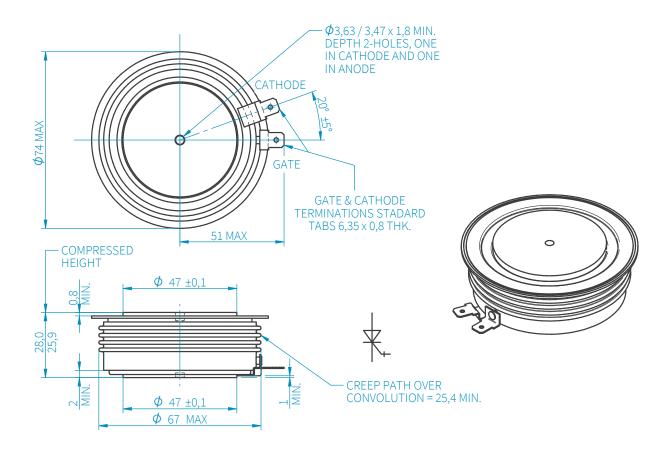
	PARAMETER	TEST CONDITIONS	MIN	ТҮР	МАХ	UNITS
V _{TM}	Maximum peak on-state voltage	I _G = 2A, I _T = 1200A	-	3.0	3.3	V
ΙL	Latching current	T _i = 25°C	-	15	-	А
Ι _Η	Holding current	1j - 25 C	-	15	-	А
(dv/dt) _{cr}	Critical rate of rise of off-state voltage	$V_{D} = 80\% V_{DRM}, V_{GR} = -2V$	1000	-	-	V/µs
I _{DRM}	Peak off-state current	Rated V_{DRM} , $V_{GR} = -2V$	-	-	50	mA
I _{RRM}	Peak reverse current	Rated V _{RRM}	-	-	100	mA
I _{GKM}	Peak negative gate leakage current	$V_{GR} = -16V$	-	-	200	mA
		$T_j = -40^{\circ}C$, $V_D = 25V$, $R_L = 25m\Omega$	-	1.0	-	V
V _{GT}	Gate trigger voltage	T_j = 25°C, V_D = 25V, R_L = 25m Ω	-	0.9	-	V
		$T_j = 125^{\circ}C$, $V_D = 25V$, $R_L = 25m\Omega$	-	0.8	-	V
		T_j = -40°C, V_D = 25V, R_L = 25m Ω	-	3.0	8.0	А
I _{GT}	Gate trigger current	$T_j = 25^{\circ}C, V_D = 25V, R_L = 25m\Omega$	-	0.6	2.5	А
		$T_j = 125^{\circ}C$, $V_D = 25V$, $R_L = 25m\Omega$	-	60	500	mA
t _d	Delay time	(note 2)	-	1.0	-	μs
t _{gt}	Turn-on time	Conditions as for $t_d, (10\% l_{GM} \mbox{ to } 10\% V_D)$	-	3.0	7.0	μs
t _f	Fall time	(note 3)	-	0.8	-	μs
t _{gq}	Turn-off time	Conditions as for t_f , (10%I_GQ to 10%I_TGQ)	-	12	13	μs
I _{GQ}	Turn-off gate current	Conditions as for t _f	-	250	-	А
Q_{GQ}	Turn-off gate charge	Conditions as for t _f	-	1600	2000	mC
t _{tail}	Tail time	Conditions as for $t_{f},(10\% I_{TGQ}$ to I_{TGQ} < 1A)	-	40	60	μs
t _{gw}	Gate off-time (note 4)	Conditions as for t _f	150	-	-	μs
		Double side cooled	-	-	0.027	K/W
R _{thJK}	Thermal resistance, junction to sink	Cathode side cooled	-	-	0.070	K/W
		Anode side cooled	-	-	0.045	K/W
F	Mounting force	(note 5)	15	-	25	kN
Wt	Weight		-	480	-	g
note 1)	Unless otherwise indicated T _j = 125°C					
note 2)	$V_D = 50\% V_{DRM}$, $I_{TGQ} = 1200A$, $I_{GM} = 40A$, $di_G/dt = 20A/\mu s$, $T_j = 25^{\circ}C$, $di/dt = 300A/\mu s$, $(10\% I_{GM} to 90\% V_D)$					
note 3)	$V_{\rm D}$ = 80% $V_{\rm DRM}$, $I_{\rm TGQ}$ = 1200A, $C_{\rm S}$ = 3 μ F, di _G /dt = 40A/ μ s, $V_{\rm GR}$ = –16V, (90% $I_{\rm TGQ}$ to 10% $V_{\rm D}$)					
note 4)	The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the pas- sage of tail current.					
note 5)	For other clamping forces, consult factory.					

Request full technical data sheet via e-mail, free of charge:

Order Now!

SANCONA[®]

Outline Drawing





SANCONA GmbH

An der Hebemärchte 26 D-04316 Leipzig // Registry Court: Leipzig HRB 32946
VAT Reg No.: DE308741810
Tax number: 232/118/085686

The information contained herein is confidential and is protected by Copyright. The information may not be used or disclosed except with written permission of and in the manner permitted by the proprietors SANCONA GmbH. In the interest of product improvement, SANCONA reserves the right to change specifications at any time without prior notice. Devices with a suffix code (2-letter, 3-letter or letter/digit/letter combination) added to their generic code are not necessarily subject to the conditions and limits contained in this report.

©SANCONA GmbH