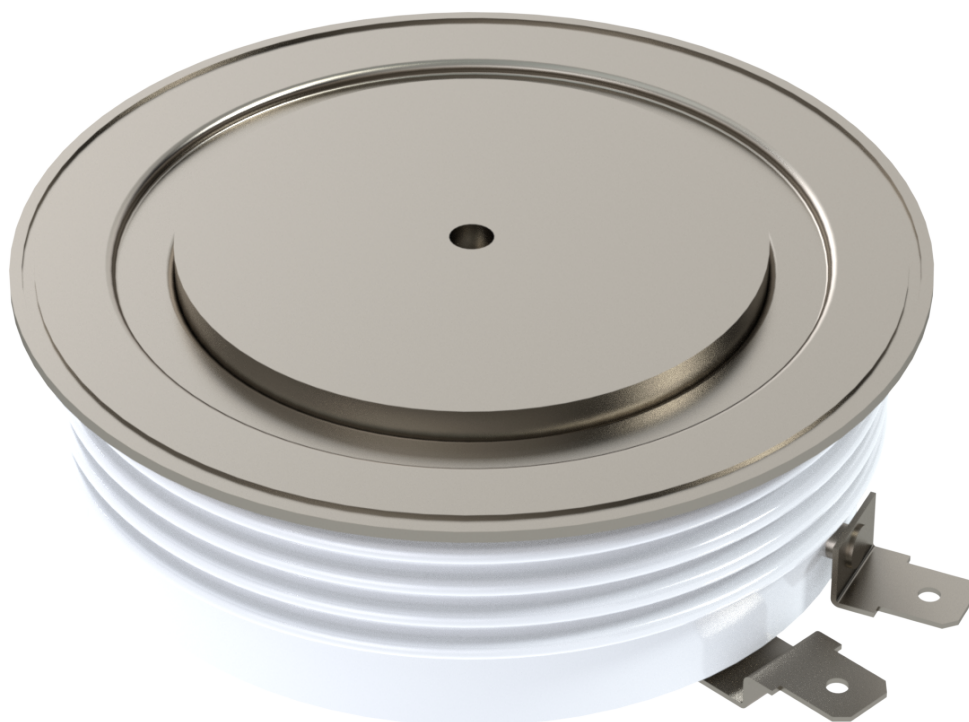


# Symmetrical Gate Turn-Off Thyristor Type SA25AP1200UN

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Date: June, 2020  
Data Sheet Issue: 1



## ORDERING INFORMATION

(Please quote 12 to 15 digit code as below)

SA	25	AP	1200	U	N	
-	Voltage Code	Outline Code	Current code	Type code	Special code	Optional code

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## Absolute Maximum Ratings

VOLTAGE RATINGS		MAXIMUM LIMITS	UNITS
$V_{DRM}$	Repetitive peak off-state voltage, (note 1)	2500	V
$V_{RSM}$	Non-repetitive peak off-state voltage, (note 1)	2600	V
$V_{RRM}$	Repetitive peak reverse voltage	875	V
$V_{RSM}$	Non-repetitive peak reverse voltage	875	V
note 1)	$V_{GK} = -2V$		

OTHER RATINGS		MAXIMUM LIMITS	UNITS
$I_{TGQ}$	Peak turn-off current (note 1)	1200	A
$L_S$	Snubber loop impedance, $I_{TM} = I_{TGQ}$ (note 1)	0.3	$\mu H$
$I_{T(AV)M}$	Mean on-state current, $T_{sink} = 55^\circ C$ , (note 2)	670	A
$I_{T(RMS)}$	Nominal RMS on-state current, $T_{sink} = 25^\circ C$ (note 2)	1340	A
$I_{TSM}$	Peak non-repetitive surge current $t_p = 10ms$	10.5	kA
$I_{TSM2}$	Peak non-repetitive surge current (note 3)	19	kA
$I^2t$	$I^2t$ capacity for fusing $t_p = 10ms$	$550 \cdot 10^3$	$A^2s$
$(di/dt)_{cr}$	Critical rate of rise of on-state current, (note 4)	1000	$A/\mu s$
$P_{FGM}$	Peak forward gate power	210	W
$P_{RGM}$	Peak reverse gate power	8	kW
$I_{FGM}$	Peak forward gate current	140	A
$V_{RGM}$	Peak reverse gate voltage (note 5)	18	V
$t_{off}$	Minimum permissible off-time, $I_{TM} = I_{TGQ}$ (note 1)	80	$\mu s$
$t_{on}$	Minimum permissible on-time	20	$\mu s$
$T_{jop}$	Operating temperature range	-40 to +125	$^\circ C$
$T_{stg}$	Storage temperature range	-40 to +150	$^\circ C$
note 1)	$T_j = 125^\circ C$ , $V_D = 80\%V_{DM}$ , $V_{DM} \leq V_{DRM}$ , $di_{GQ}/dt = 20A/\mu s$ , $C_S = 3\mu F$		
note 2)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Half-sinewave, $t_p = 2ms$		
note 4)	For $di/dt > 1000A/\mu s$ please consult factory.		
note 5)	May exceed this value during turn-off avalanche period.		

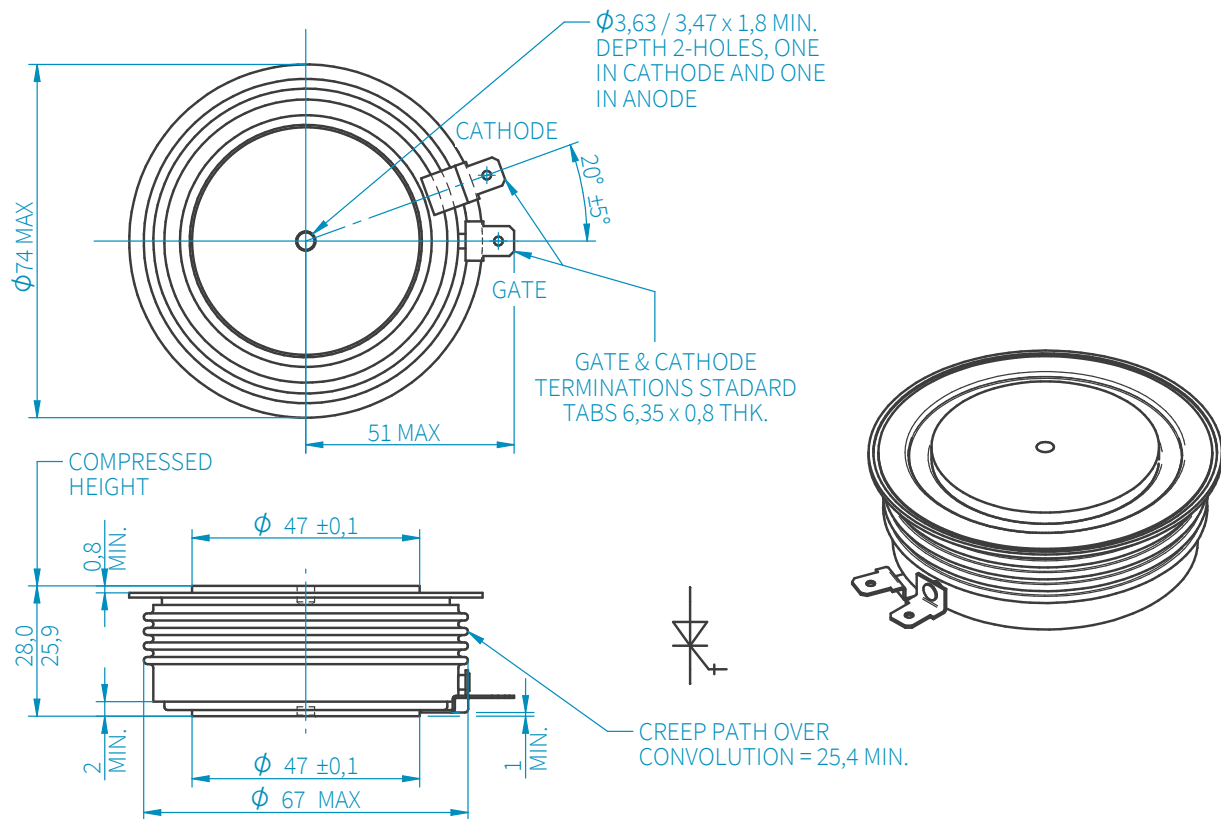
## Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
$V_{TM}$	Maximum peak on-state voltage	$I_G = 2A, I_T = 1200A$		-	3.0	3.3	V
$I_L$	Latching current	$T_j = 25^\circ C$		-	15	-	A
$I_H$	Holding current			-	15	-	A
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	$V_D = 80\%V_{DRM}, V_{GR} = -2V$		1000	-	-	V/ $\mu s$
$I_{DRM}$	Peak off-state current	Rated $V_{DRM}, V_{GR} = -2V$		-	-	50	mA
$I_{RRM}$	Peak reverse current	Rated $V_{RRM}$		-	-	100	mA
$I_{GKM}$	Peak negative gate leakage current	$V_{GR} = -16V$		-	-	200	mA
$V_{GT}$	Gate trigger voltage	$T_j = -40^\circ C, V_D = 25V, R_L = 25m\Omega$		-	1.0	-	V
		$T_j = 25^\circ C, V_D = 25V, R_L = 25m\Omega$		-	0.9	-	V
		$T_j = 125^\circ C, V_D = 25V, R_L = 25m\Omega$		-	0.8	-	V
$I_{GT}$	Gate trigger current	$T_j = -40^\circ C, V_D = 25V, R_L = 25m\Omega$		-	3.0	8.0	A
		$T_j = 25^\circ C, V_D = 25V, R_L = 25m\Omega$		-	0.6	2.5	A
		$T_j = 125^\circ C, V_D = 25V, R_L = 25m\Omega$		-	60	500	mA
$t_d$	Delay time	(note 2)		-	1.0	-	$\mu s$
$t_{gt}$	Turn-on time	Conditions as for $t_d$ , (10% $I_{GM}$ to 10% $V_D$ )		-	3.0	7.0	$\mu s$
$t_f$	Fall time	(note 3)		-	0.8	-	$\mu s$
$t_{gq}$	Turn-off time	Conditions as for $t_f$ , (10% $I_{GQ}$ to 10% $I_{TGQ}$ )		-	12	13	$\mu s$
$I_{GQ}$	Turn-off gate current	Conditions as for $t_f$		-	250	-	A
$Q_{GQ}$	Turn-off gate charge	Conditions as for $t_f$		-	1600	2000	mC
$t_{tail}$	Tail time	Conditions as for $t_f$ , (10% $I_{TGQ}$ to $I_{TGQ} < 1A$ )		-	40	60	$\mu s$
$t_{gw}$	Gate off-time (note 4)	Conditions as for $t_f$		150	-	-	$\mu s$
$R_{thJK}$	Thermal resistance, junction to sink	Double side cooled		-	-	0.027	K/W
		Cathode side cooled		-	-	0.070	K/W
		Anode side cooled		-	-	0.045	K/W
F	Mounting force	(note 5)		15	-	25	kN
$W_t$	Weight			-	480	-	g
note 1)	Unless otherwise indicated $T_j = 125^\circ C$						
note 2)	$V_D = 50\%V_{DRM}, I_{TGQ} = 1200A, I_{GM} = 40A, di_G/dt = 20A/\mu s, T_j = 25^\circ C, di/dt = 300A/\mu s, (10\%I_{GM} \text{ to } 90\%V_D)$						
note 3)	$V_D = 80\%V_{DRM}, I_{TGQ} = 1200A, C_S = 3\mu F, di_G/dt = 40A/\mu s, V_{GR} = -16V, (90\%I_{TGQ} \text{ to } 10\%V_D)$						
note 4)	The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the passage of tail current.						
note 5)	For other clamping forces, consult factory.						

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## Outline Drawing



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